

## ABSTRACT

1       An debug and emulation system includes a target device  
2 embodied in a single integrated circuit. The target device  
3 includes a function clock circuit and an operation circuit  
4 operating in synchronism with the function clock. A trace  
5 trigger circuit triggers trace operation upon detection of a  
6 predetermined condition within the operation circuit. A FIFO  
7 buffer receives the trace data which is exported via a trace  
8 port. The integrated circuit includes an oscillator clock  
9 circuit which may be synchronized with the function clock or  
10 a reference clock. The trace trigger circuit and the FIFO  
11 input operate on the function clock. The FIFO output and the  
12 trace port operate on the oscillator clock. Thus the trace  
13 may operate all on the function clock or be split between the  
14 function clock and the reference clock. The trace data is  
15 sensed in synchronism with the oscillator clock. The emulator  
16 is coupled to the target device to control the clock  
17 selection. Accordingly, the trace export can operate at a  
18 frequency independent of the operation circuit.